REMARKS

In response to the Official Action:

[2] The specification was objected to for lack of antecedent basis for " a gate connected to a first-conductivity-type layer under a gate of said second-conductivity-type MOS output transistor." This objection is respectfully traversed.

The objected-to phrase occurs in claim 16, exemplified in Fig. 3. The lower half of Fig. 3 follows Fig. 1, while the upper half of Fig. 3 is a complementary structure. The two complementary structures are described by the second and third paragraphs of claim 16, and these paragraphs are interchangeable by switching "first" and "second". Because of this symmetry, the upper and lower portions of Fig. 3 are supported by the same disclosure (page 11, lines 6-10 in the specification). In particular, Fig. 1 and its description apply equally to both the upper and the lower portions of Fig. 3, and to both the second and the third paragraphs of claim 16. Thus, Fig. 1 can support both the third paragraph of claim 16 (including the objected-to language) and the second paragraph of claim 16 (including complementary language not objected to).

Figs. 1(a) and 1(b) show that the second-conductivity-type (i.e., NMOS) MOS protection transistor 10 has a gate 14 connected to a first-conductivity-type (P type) layer 22 under a gate 21 of the second-conductivity-type MOS output transistor 11. Page 10, line 13 of the specification states that "A gate electrode 14 of the NMOS dummy transistor 10 is connected to the P-well 22 via the P+ contact layer 27 of the NMOS output transistor 11."

The passage at page 10, line 13 is believed to overcome the objection. However, if the Examiner deems it does not, then clarification is requested.

[3-4] Claims 5 and 31-32 were rejected under §102(e) as being anticipated by Ker '529. This rejection is respectfully traversed.

Claim 32, as now amended and exemplified in the description, reads as follows:

A semiconductor apparatus [Figs. 1-3] *comprising:*

an output electrode [12] *from which an output signal of the semiconductor apparatus is output;*

a first-conductivity-type MOS output transistor [11] *respectively including a drain electrode* [upper terminal in Fig. 1(a); 25 in Fig. 1(b)] *connected to the output electrode* [12], *a source electrode* [26] *connected to a ground voltage terminal* [13], *a gate electrode* [21] *connected to a signal line* [24], *and a second-conductivity-type layer* [22 in Fig. 1(b)] *located under the gate electrode* [21], *wherein the first-conductivity-type MOS output transistor transmits the output signal of the semiconductor apparatus to the output electrode responsive to a signal on the signal line* [24]*;*

a first-conductivity-type MOS protection transistor [10] *respectively including a drain electrode* [upper terminal in Fig. 1(a); 15 in Fig. 1(b)] *connected to the output electrode* [12], *a source electrode* [lower terminal in Fig. 1(a); 16] *connected to the ground voltage terminal* [13], *and a gate electrode* [heavy vertical line in Fig. 1(a); 14 in Fig. 1(a)] *connected to the ground voltage terminal* [13]*; and*

a metallic wiring member [28, amended Fig. 1(b)] *which connects the second-conductivity-type layer* [22] *of the first-conductivity-type MOS output transistor to the gate electrode* [14] *of the first-conductivity-type MOS protection transistor* [10];

wherein said first-conductivity-type MOS output transistor [11] *further includes a second-conductivity-type + area* [27] *which is formed in said second-conductivity-type layer* [22] *and substantially surrounds said drain electrode* [25] *and said source electrode* [26].

The subject matter of the last paragraph is illustrated in Fig. 2, as explained above on the first page of this paper and in the amended specification. The advantages are explained below.

Low Resistance of "+". In the specification, the layer 22 is described as a P-well and the area 27 is said to be P+, meaning that there is more doping in the area 27 than in the rest of the layer 22. Because there is more doping, there is also better electrical conduction in the area 27 than in the rest of the layer 22.

The specification at page 10, line 13, states: "A gate electrode 14 of the NMOS dummy transistor 10 is connected to the P-well 22 via the P+ contact layer 27 of the NMOS output transistor 11, and a gate electrode 21 of the NMOS output transistor 11 is connected to an output signal line 24. Here, the gate electrode and the P-well are preferably directly connected by a wiring *and the like* and not via another well. This is because, if connected via a well, the high well resistance would be inserted" (emphasis added). The Examiner is invited to note that "and the like" can only refer to the area 27, which is non-metallic but, like wiring, relatively conductive. Thus, the specification supports the use of a "+" area for electrical connection without "high resistance."

Further support is found at page 14, line 6, stating, "in order to connect the gate electrode to the P- area, it is preferable that ... a P+ area 51 [is] connected to the area of the P-diffusion layer 45 [and] the gate electrode is connected via a electrode wiring to the P+ area 51. With this configuration, the gate electrode 41 of the protection transistor can be connected to the P- diffusion layer 45 without increasing connection resistance."

Conduction and Dummy Gate Voltage. When a breakdown occurs in the first-conductivity-type MOS output transistor 11, the resulting potential rise in the second-conductivity-type layer 22 is more effectively transmitted to the gate electrode 14 of the first-conductivity-type MOS protection transistor 10 due to the + type material in the claimed area 27 of the layer 22.

The specification at page 13, line 9, states, "by connecting the gate of the dummy transistor, which is high in ESD resistance and later in breakdown, to the *Body region of the output transistor*, which is low in ESD resistance and earlier in breakdown, when breakdown

due to an ESD surge occurs earlier in the output transistor, the *gate potential of the dummy transistor* rises in conjunction with the rise of the Body potential. Thus, with the ON-current of the dummy transistor flowing, the surge current does not concentrate in the output transistor, thereby protecting the output transistor" (emphasis added).

Ker. Ker discloses neither the new feature nor the advantage gained from it. The Examiner 10 (page 5, line 6) points to Ker's Fig., showing a P+ area (coupled to VSS) in a P-well. However, this P+ area is not disclosed to substantially surround anything at all, much less the drain and source electrodes as is now claimed.

[5-6] Claims 2, 3, and 6-30 were rejected under §103 as being unpatentable over Ker and Staab '790. This rejection is respectfully traversed on the grounds set out above and further on lack of disclosure in Staab of the new feature in the independent claims.

Withdrawal of the rejections, and allowance of the remaining claims, is requested.

Respectfully submitted,

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Date

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